RESEARCH DEPARTMENT

Up-conversion by means of a line-store standards converter using a line-delay interpolator

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SUMMARY

This report is concerned with the conversion of 405-line television signals to 625-line signals using a line-store standards converter incorporating a line-delay interpolator. The basic operations carried out on the video signals in such a converter are described and an outline is given of the circuit arrangements required to control these operations.

1. INTRODUCTION

The basic principles of line-store standards conversion using a line-delay interpolator have already been described elsewhere.[1,2,3,4] In this report, the operation of a 405- to 625-line converter is considered in more detail. Although 405- to 625-line conversion is the particular case considered, many of the principles described may be generally applied to "up-conversions" from one standard to another having a greater number of lines, assuming that both standards have the same number of fields per second.

The following abbreviations are used throughout the report:-

T_i represents the duration of one line-period of the input standard

T_0 represents the duration of one line-period of the output standard

2. OUTLINE OF OPERATION OF CONVERTER

A block diagram of a line-store standards converter using a line-delay interpolator is shown in Fig. 1. This diagram applies only to up-conversion; for down-conversion, the interpolating section would precede the time-redistributing store.

The method of operation of the converter is as follows:

The time-redistributing store redistributes the information contained in each input line-period so that it occupies one output line-period. The resulting output signal from the store during 405- to 625-line conversion contains video information during 405 of the 625 lines in each picture period, and there is no video information during the remaining 220 lines. This is inevitable since reading destroys the stored information in the type of store used. Information is provided during the 220 blank lines by repeating information from preceding line-periods. This process is performed by the delay unit which also has the function of providing information derived from two successive input lines during each output line interval.

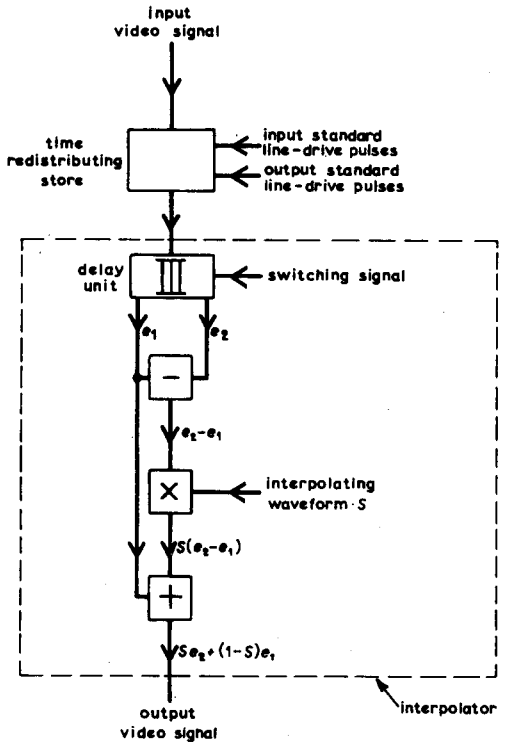

Fig. 1 - Block diagram of converter

The interpolating section of the converter processes the output signal from the delay unit and provides each output line with a video signal which is suited to its vertical position in the picture. This information is obtained by adding suitable proportions of the video signals derived from the two input lines which, spatially, lie immediately above and below the position of an output line. This interpolation process can be expressed in the form of an equation.

$$e = Se_2 + (1-S)e_1 \qquad (1)$$

where e is the signal representing a required output line and e_1 and e_2 are signals representing the two input lines which, in spatial terms, lie on either side of this output line. "S" is known as the interpolation function and its value depends upon the position, measured in the direction of field scanning, of the output line relative to the position of the two input lines. One possible relationship between S and the relative positions of input and output lines is shown in Fig. 2.[5]

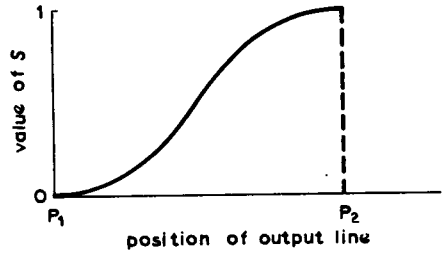

Fig. 2 - Variation of interpolation function S with position of output line

P_1 and P_2 indicate positions of two successive input lines which lie on either side of output line, distance being measured in direction of field scanning.

Since the signals e_1 and e_2 appear at the output of the store at different times, it is necessary to delay one of these signals relative to the other so that they are made available simultaneously. This process is carried out in the delay unit shown in Fig. 1.

The required output signal "e", defined by Equation (1), is obtained from the signals e_1 and e_2 by processing these signals in the subtractor, modulator and adder units shown in Fig. 1. The interpolation function signal fed to the modulator is derived from the input and output synchronizing pulses; its generation will be described in Section 5.4.

3. OPERATION OF THE TIME-REDISTRIBUTING STORE

This section describes the basic principles governing the operation of the redistributing store, the detailed design of which is discussed in References 3 and 6. This store redistributes the information contained in each input line-period so that it occupies one output line-period. In order to carry out this operation, the input signal is sampled approximately 600 times during each line-period and these samples are written consecutively into 600 separate capacitor stores. The samples stored in the capacitors are then read out at a suitable rate during one output line-period.

The time-redistributing store is designed so that the n^{th} sample of each line-period is stored in the same capacitor; the information handled by a given capacitor therefore corresponds to a vertical strip of picture approximately one picture element in width. Further, the reading process destroys the information contained in the stores.

A typical sequence of writing and reading actions during several successive lines is illustrated by the diagram shown in Fig. 3. The solid diagonal lines C,D,E etc. indicate the times at which input information is written in to the stores

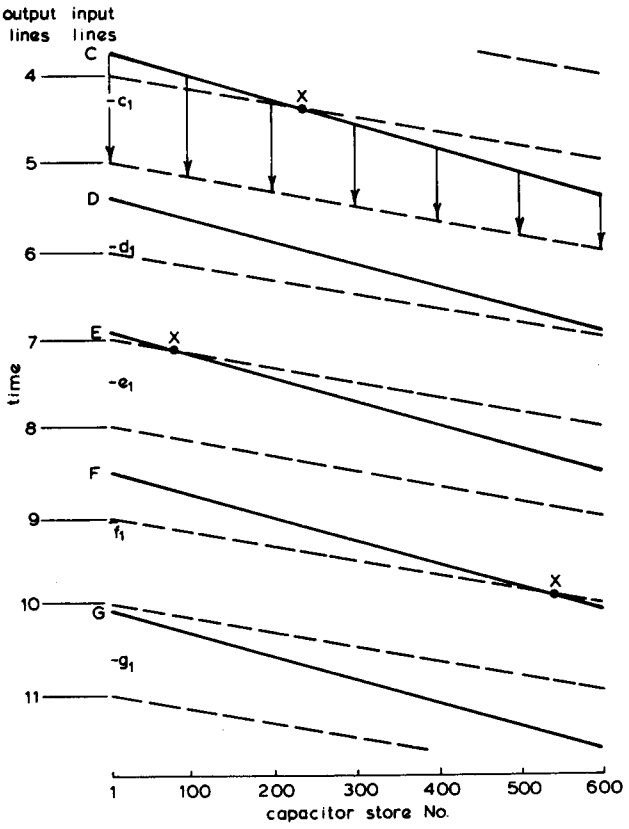

Fig. 3 - Times at which writing and reading (if not inhibited) take place at each capacitor in redistributing store

——— Writing of input signal

— — — Reading of output signal

and the broken diagonal lines 4,5,6 etc. indicate the times at which reading occurs. In practice writing and reading only occur during the part of each line-period containing video information, but in this report the effects of line blanking have been ignored.

If reading is allowed during each output line, then instrumental difficulties arise due to the fact that the reading process overtakes the writing process during some input line-periods (e.g. during input lines C,E,F, etc.). This problem is overcome by inhibiting the reading process during the whole of each output line-period in which write/read "crossovers" would otherwise occur.

A decision can be made at the beginning of each output line as to whether reading should be allowed to occur by using the fact that crossovers occur during output lines which start less than $T_i - T_0$ after the start of an input line. An output line starting at the same time as an input line will cause a crossover at the first store; an output line ending at the same time as an input line (i.e. the output line starts $T_i - T_0$ after the input line) will cause a crossover at the last store. Referring to Fig. 3, reading is only allowed during output lines which start within the intervals c_1D, d_1E, e_1F, etc. Since these intervals are each of duration T_0, there will always be one, and only one, output line starting within each of these intervals, and therefore, reading and writing take place alternately at each capacitor. The information written during input line C, for example, would be read out during output line 5, no information being read out during line 4; in the diagram the transference of information is indicated by vertical arrowed lines.

If reading is inhibited in the manner described above, the input video signal is transferred to 405 out of the 625 lines in each picture-period of the output standard. This is because writing and reading now occur alternately at each capacitor store and 405 "reads" result from 405 "writes".

If the waveform representing the input signal to the store is as shown in Fig. 4(*a*), then the waveform representing the output signal from the store will be as shown in Fig. 4(*b*). Output line 5 is marked C′ to indicate that it contains the information of input line C; other output lines are marked so as to indicate the input lines from which their information is derived.

4. OPERATION OF DELAY UNIT AND INTERPOLATOR

4.1. Determination of Required Signal Delays

This section describes the processes carried out in the interpolating section of the converter. The need for interpolation arises because output lines do not scan exactly the same horizontal strips of the picture as the input lines and the purpose of this section of the converter is to provide each output line with video information suited to its particular vertical position in the picture. As outlined in Section 2, information for each output line is obtained by adding suitable proportions of the video signals from the two input lines which, spatially, lie immediately above and below the position of that output line. In the case of conversion to a higher number of lines, information from some pairs of consecutive input lines needs to be combined in two different ratios to provide video signals for the two output lines which lie between them.

The first step in the interpolation process is to obtain simultaneous information from two successive input lines during each output line. In 405- to 625-line conversion, the required information for each output line is always available when needed if the output of the store is delayed by 1, 2 and 3 output line-periods. The process of selecting the correct delayed signals from which each output line will be formed is illustrated in Fig. 5. The two patterns shown in columns 1 and 2 of Fig. 5 indicate the relative times at which input and output lines

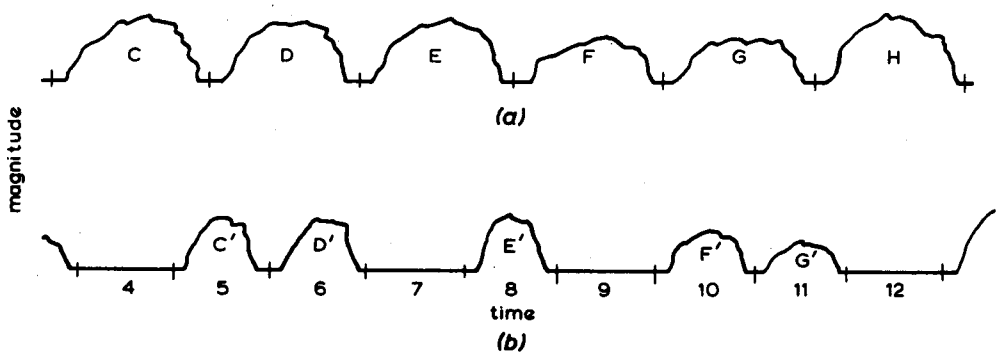

Fig. 4
Typical input and output video signals of redistributing store
(*a*) Input video signal
(*b*) Output video signal

start. As explained previously, the output signal from the store only contains video information during the lines marked C′, D′, E′, etc. and the dotted lines between D′ and E′, E′ and F′, etc. represent output line-periods during which no video signal is directly available from the store.

The column headed "delay" indicates the minimum delays, in multiples of T_0, required to provide information from two successive input lines during each output line. The resulting information obtained during each output line is indicated under column 4 in Fig. 5; for example, the video signals D′ and E′ are available during output line 9, E′ and F′ during output line 10, etc.

Since output line 9 is to be derived from video signals D′ and E′, it follows that the video information on line 9 must represent picture detail along a line lying between input lines D and E. Similarly, line 10 lies between input lines E and F and so on. Proceeding in this way, it can be seen that if the displays of the input and output signals of the converter were superimposed in such a way that the picture information in the two displays coincided, then the relative positions of input and output lines would be similar to that indicated by the relative positions of the lines in columns 4 and 5 of Fig. 5. The manner in which the two signals available during each output line are combined to form the final output signal of the converter is discussed in Section 4.4.

4.2. Delay Systems for Up-Conversion between Standards having any Number of Lines per Field

Fig. 5 shows that when the output signal from the store is delayed by a cascade of delays, each of duration T_0, the video signal derived from the input is made available to a number of output lines. In general, a delay of integral multiples of T_0 up to

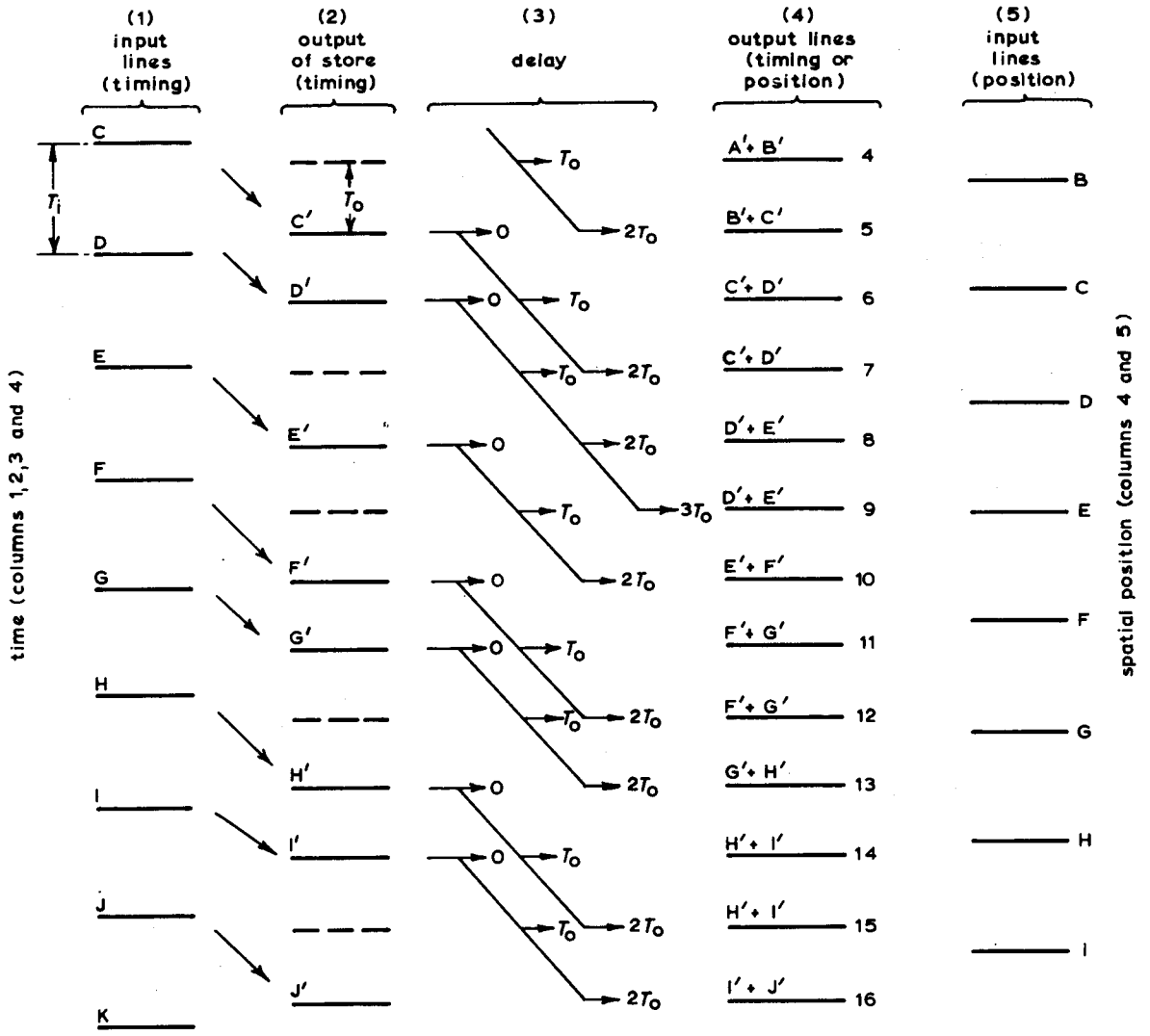

Fig. 5 - Delay-line switching sequence for 405/625-line conversion

NT_0 makes a given input line available for N output line-periods. The action of the store adds a further output line-period thus making the input line available during a total interval of $(1 + N)T_0$.

When interpolation is carried out between successive pairs of input lines, as described later in this report, then the information from any input line is required for those output lines starting within an interval of $2T_i$. Since the interval during which the video information from an input line is available must be greater than the interval during which it is required, it is necessary that:

$$(1 + N)T_0 \geqslant 2T_i$$

$$\text{or } N \geqslant (2T_i/T_0) - 1 \qquad (2)$$

Equation (2) gives the minimum total amount by which the output of the store must be delayed if suitable signals for interpolation are to be available during all output lines. For 405- to 625-line conversion, equation (2) gives $N \geqslant 2{\cdot}08$ and therefore, since N is an integer, three delays of T_0 are required for this conversion.

4.3. Instrumentation of Delay Systems suitable for a 405- to 625-line Converter

One possible arrangement for providing suitable information for interpolation during each output line is shown in Fig. 6(*a*). The two signals required during each output line are obtained from switches S1 and S2. While this delay system is the most obvious method of obtaining suitable signals for interpolation, it is not always used in practice since it is also possible to obtain the required signals by using only two delay lines. Various systems using two delay lines have been examined and the system which offers the greatest saving in cost and complexity without compromise in performance is shown in Fig. 6(*b*). In this system the output of the one-line delay is recirculated back to the input of both delays during the "blank" line-periods from the store, thus ensuring that video signals are present at their inputs at all times. S4 is operated at the same times as S3, so that e_2 is obtained from the output of the two-line delay during blank lines from the store, and from the one-line delay during the remaining line-periods. The requirement for a delay of $3T_0$ is satisfied when the one-line and two-line delays operate in series.

4.4. The Interpolator

It is assumed in the interpolation process that the positions of the output lines are parallel to the positions of the lines scanned by the input

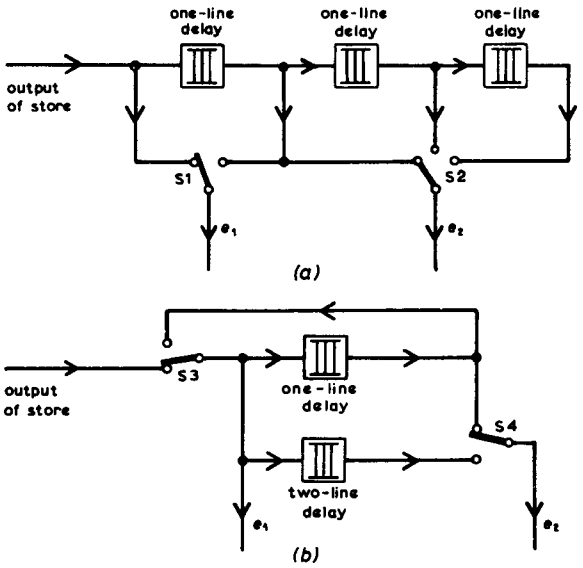

Fig. 6 - Delay systems for 405/625-line conversion

(a) System using 3 delay lines
(b) System using 2 delay lines

standard. This assumption is made to avoid practical difficulties which would arise if it were assumed that output lines could cross input lines, as would occur if normal 405- and 625-line rasters were superimposed. Interpolating in this manner is known as "parallel" interpolation and its only disadvantage is that it causes a very small geometrical distortion of objects in a display of the output signal. For example, a rectangular object would appear as a parallelogram with corners of $90° \pm 0{\cdot}07°$.

With parallel interpolation, the whole of each output line is derived from the same pair of input lines and the value of the interpolation function S is kept constant during any given output line.

As described in Section 2, the ratios in which the two video signals available during each output line-period are combined to form the interpolated output signal are determined from the spatial relationships of lines on superimposed rasters of the input and output standards. It is not possible to base these ratios upon the actual input and output rasters because input signals are delayed before reaching the interpolator. A vertically displaced version of the input raster must be assumed in deriving the interpolating waveform and the position of this hypothetical raster is indicated in column 5 of Fig. 5. It can be shown that the exact position of a line in column 5 should be opposite a point lying $2T_i - T_0$ below the corresponding line in column 1. As an example, line C in column 5 is opposite a point lying $2T_i - T_0$ below line C (or $T_i - T_0$ below line D) in column 1. This relation-

ship between the "timing" and "position" of input lines is used in the generation of the interpolation waveform (see Section 5.4.).

Having established the relative positions of input and output lines, the ratio in which the two available video signals should be combined during each output line can be determined from the interpolation law (see Fig. 2).

Reference 2 discusses the preferred arrangement of units for performing this task. In effect the difference between the two given video signals is multiplied by the interpolating function and added to the least-delayed signal. The instrumentation of the subtractor, adder and multiplier shown in the interpolator section of Fig. 1 is straightforward and apart from requiring considerable precision presents no special problems.

5. DERIVATION OF CONTROL AND INTERPOLATION WAVEFORMS

5.1. General

The purpose of this section is to give a brief outline of the method of operation of some of the control circuits required in the conversion processes described in the previous sections of this report.

The circuits considered provide the following:

(*a*) A waveform which will cause the reading action in the redistributing store to take place during only those output line-periods which start at least $T_i - T_0$ after the start of the previous input line-period.

(*b*) A waveform which will operate the switches in the delay network at the required times.

(*c*) A waveform corresponding to the interpolation function S.

All the above waveforms may be derived from input and output line-drive pulses.

Typical waveforms for the three requirements are shown in Fig. 7 and a block diagram of the basic circuits used to derive them is shown in Fig. 8.

The circuits described have been somewhat simplified by ignoring precautions taken to avoid difficulties which arise when input and output line synchronizing pulses occur almost simultaneously.

5.2. Generation of a Waveform that is Required to Indicate Output Lines During which Information is to be Read from the Store

Figs. 7(*a*) and (*b*) show the relative starting times of input lines C, D, E, etc. and output lines 4, 5, 6, etc. The intervals Cc_1, Dd_1, Ee_1, etc. are equal to $T_i - T_0$. As explained previously, reading should only take place in the redistributing store during those output line-periods which start within the intervals c_1D, d_1E, e_1F, etc., that is, during the output lines indicated in Fig. 7(*c*). The pulses in this waveform will be referred to as "useful" output line-drive pulses. The redistributing store is designed so that reading only takes place during the output line-period which immediately follows each of these "useful" pulses.

In order to select the "useful" pulses, it is first necessary to generate pulses which occur $T_i - T_0$ after the start of each input line-period. As shown in Fig. 8, these pulses are generated by means of a monostable circuit fed with input line-drive pulses. The delayed line-drive pulses obtained from this monostable set the bistable circuit B1 to such a state that the gate connected to its output is opened. The next output line-drive pulse to arrive at this gate after it has been opened passes through the gate and resets B1. Once B1 has been reset, the gate is closed and no more output line-drive pulses can pass until the gate has been reopened by the next input line-drive pulse. In this way only one output line-drive pulse is allowed through the gate for each input line-drive pulse. The pulses which pass through this gate indicate the start of output lines during which reading should take place.

5.3. Derivation of the Switch Control Waveform

Only the switch control waveform required for the two delay-line arrangement shown in Fig. 6(*b*) is considered as the three delay-line arrangement is not used in practice. As explained in Section 4.2, the switches must be in one position during output line-periods when information is being read out of the distributing store and in the other position during the output line-periods when no signal is read from the store. The switching waveform should therefore be of the form shown in Fig. 7(*d*).

This switching waveform is generated by feeding the original output line-drive pulses and the "useful" pulses respectively to the two inputs of bistable circuit B2 shown in Fig. 8. By choosing suitable input time-constants for this circuit, it is arranged that the bistable adopts one "state" when pulses have been applied to both inputs simultaneously and the opposite state when no "useful"

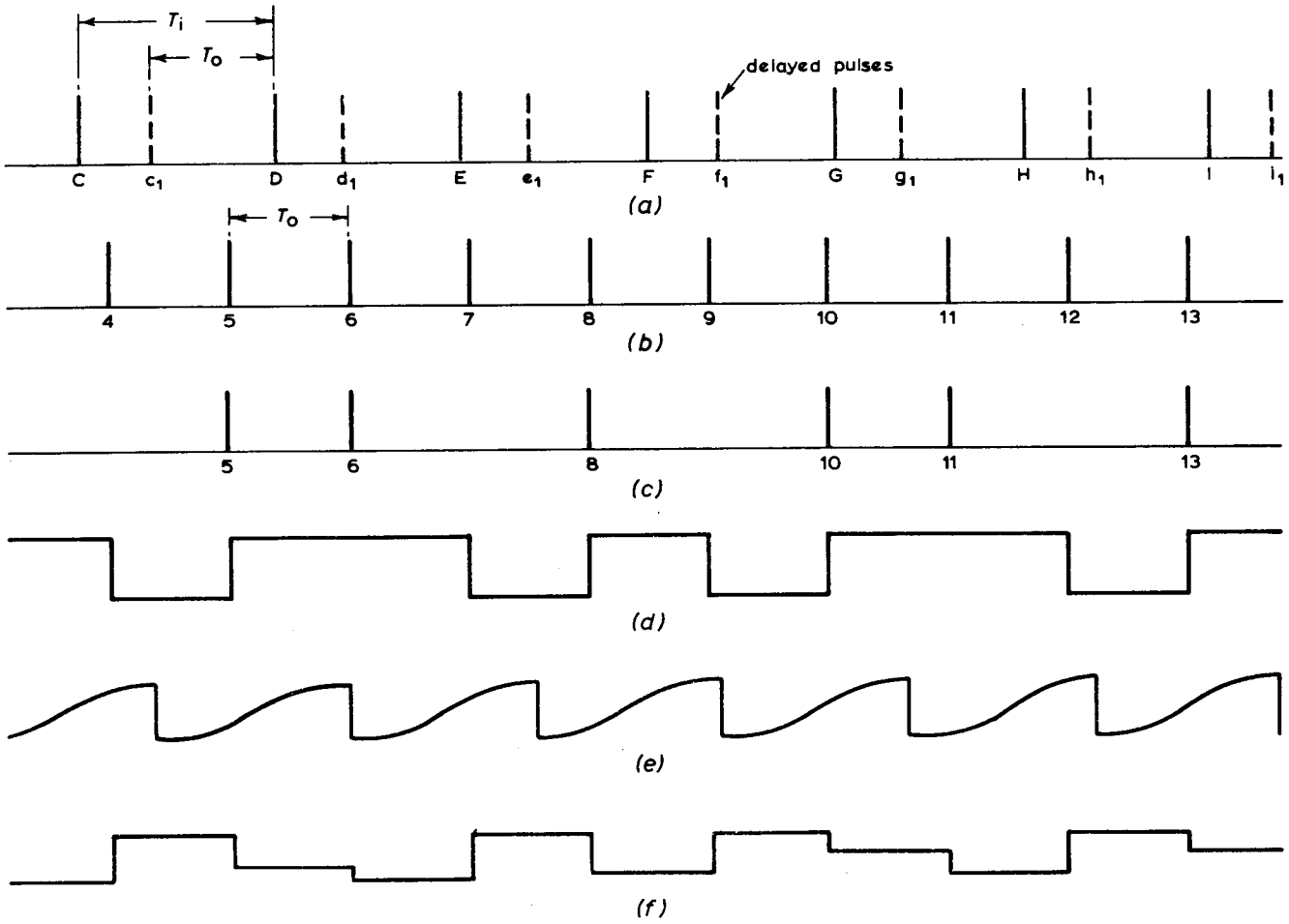

Fig. 7 - Waveforms in control and interpolation circuits

(a) Input line-drive pulses (b) Output line-drive pulses
(c) "Useful" output line-drive pulses (d) Interpolation waveform before sampling
(e) Interpolation waveform "S"

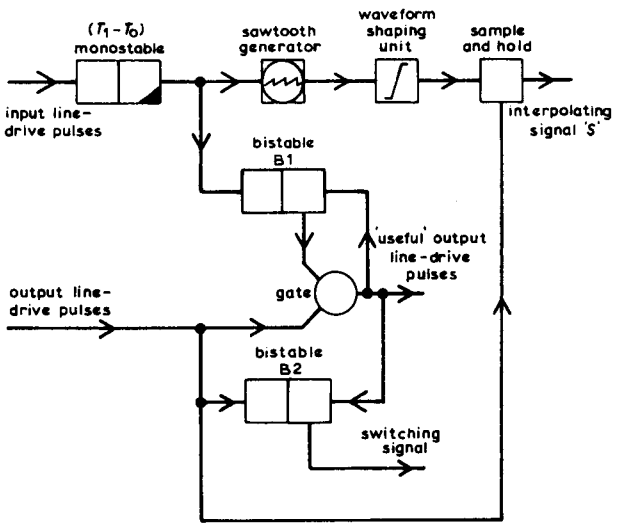

Fig. 8 - Block diagram of control and interpolation circuits

pulse has been applied to its right-hand input (Fig. 8). The resulting waveform obtained at the output of this bistable has the form required by the switching signal.

5.4. Interpolation Waveform

In order to derive a voltage whose magnitude is proportional to the value of the interpolating function S, it is first necessary to derive the waveform shown in Fig. 7(e); each cycle of this waveform starts $T_i - T_0$ after the start of an input line-period and has the same shape as the interpolating function. The waveform is obtained by shaping the output signal from a sawtooth generator which is triggered by delayed input line-drive pulses from the $T_i - T_0$ monostable circuit shown in Fig. 8. A voltage whose magnitude is proportional to the value of S required during each output line is obtained from a sample-and-hold circuit which samples the output of the waveform shaping unit

at the start of each output line-period. The result is illustrated in Fig. 7(*f*). This voltage is fed to the modulator shown in Fig. 1.

6. PERFORMANCE

A 405- to 625-line standards converter based on the principles described in this report has been constructed and found to perform adequately. The output picture quality is satisfactory but could be improved if a more complex system of interpolation were used. The use of video information from three or four consecutive lines of one field or information from two or more spatially adjacent picture lines (particularly the latter) would result in an improved performance.

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